

500V N-Channel MOSFET

General Description

This Power MOSFET is produced using advanced planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

Features

20A, 500V, $R_{DS(on)}$ typ. = 0.21Ω @ $V_{GS} = 10$ V

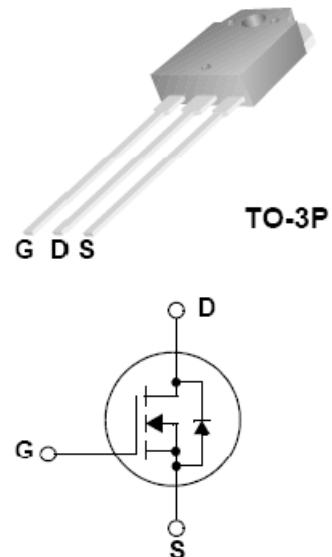
Low gate charge (50nC)

High ruggedness

Fast switching

100% avalanche tested

Improved dv/dt capability



Absolute Maximum Ratings $T_c = 25$ °C unless otherwise noted

Symbol	Parameter		JFAM20N50C	Units
V_{DSS}	Drain–Source Voltage		500	V
I_D	Drain Current	Continuous ($T_c = 25$ °C)	20*	A
		Continuous ($T_c = 100$ °C)	13*	A
I_{DM}	Drain Current - Pulsed (Note 1)		75	A
V_{GSS}	Gate – Source Voltage		± 30	V
EAS	Single Pulsed Avalanche Energy (Note 2)		450	mJ
I_{AR}	Avalanche Current (Note 1)		20	A
E _{AR}	Repetitive Avalanche Energy (Note 1)		20.7	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		50	V/ns
P_D	Power Dissipation ($T_c = 25$ °C)		280	W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum lead temperature for soldering purposes 1/8" from case for 5 seconds		300	°C

*Drain current limited by maximum junction temperature.

Thermal characteristics

Symbol	Parameter	JFAM20N60C			Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.45			°C/W
$R_{\theta JS}$	Thermal Resistance, Case-to-Sink Typ.	--			°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	40			°C/W

Electrical Characteristics $T_c = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 V, I_D = 250 \mu A$	500	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu A$, Referenced to $25^\circ C$	--	0.5	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 500 V, V_{GS} = 0 V$	--	--	1	uA
		$V_{DS} = 400 V, T_c = 125^\circ C$	--	--	10	uA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30 V, V_{GS} = 0 V$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30 V, V_{GS} = 0 V$	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source on-Resistance	$V_{GS} = 10 V, I_D = 10 A$	--	0.21	0.35	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40 V, I_D = 10 A$ (Note 4)	--	18	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 \text{ MHz}$	--	2310	--	pF
C_{oss}	Output Capacitance		--	1270	--	pF
C_{rss}	Reverse Transfer Capacitance		--	85	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DS} = 250 V, I_D = 20.0 A, R_G = 25 \Omega, V_{GS} = 10 V$ (Note 4,5)	--	63	--	ns
t_r	Turn-On Rise Time		--	135	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	210	--	ns
t_f	Turn-Off Fall Time		--	75	--	ns
Q_g	Total Gate Charge		--	56	--	nC
Q_{gs}	Gate-Source Charge	$V_{DS} = 250 V, I_D = 20.0 A, V_{GS} = 10 V$ (Note 4,5)	--	17	--	nC
Q_{gd}	Gate-Drain Charge		--	26	--	nC
Drain – Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current	--	--	20	A	
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	80	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 V, I_S = 20.0 A$	--	--	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0 V, I_S = 20.0 A$ $dI_f/dt = 100 A/\mu s$ (Note 4)	--	460	--	ns
Q_{rr}	Reverse Recovery Charge		--	5.1	--	uC

Notes:

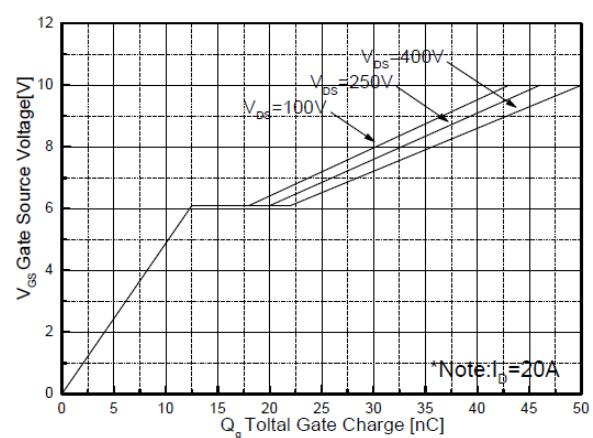
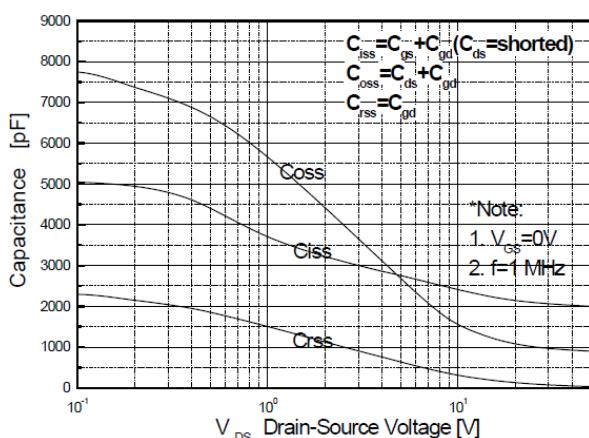
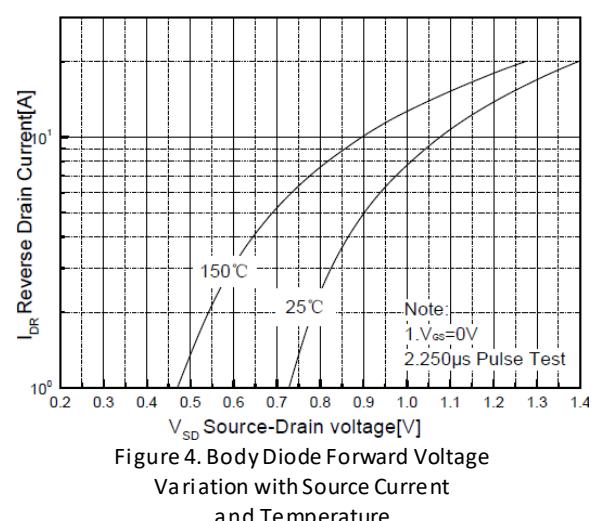
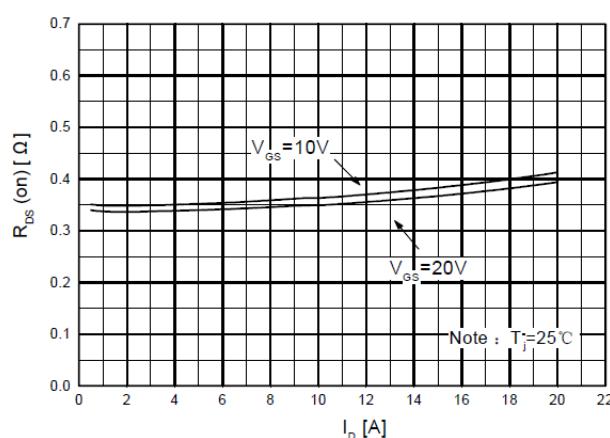
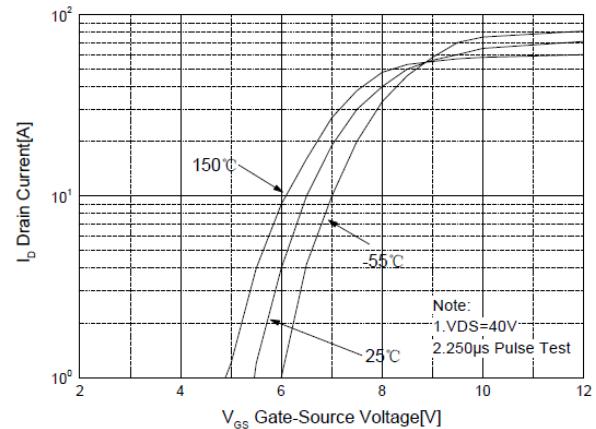
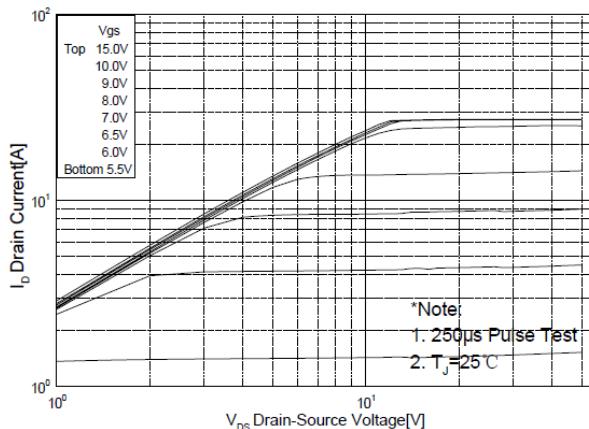
- Repetitive Rating: Pulsed width limited by maximum junction temperature
- $L = 5.0 mH, I_{AS} = 20 A, V_{DD} = 50 V, R_G = 25 \Omega$, Starting $T_J = 25^\circ C$
- $I_{SD} \leq 20.0 A, di/dt \leq 200 A/\mu s, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ C$
- Pulsed Test: Pulsed width $\leq 300 \mu s$, Duty cycle $\leq 2\%$
- Essentially independent of operating temperature

Typical Characteristics



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JFAM20N50C



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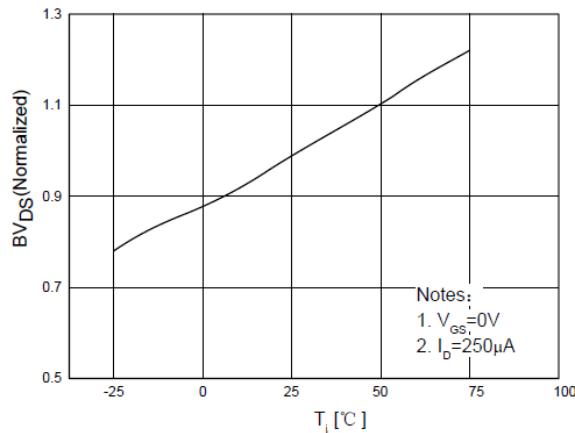


Figure 7. Breakdown Voltage Variation
vs Temperature

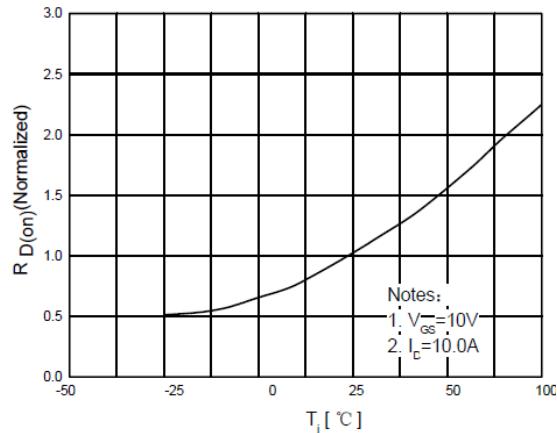


Figure 8. On-Resistance Variation
vs Temperature

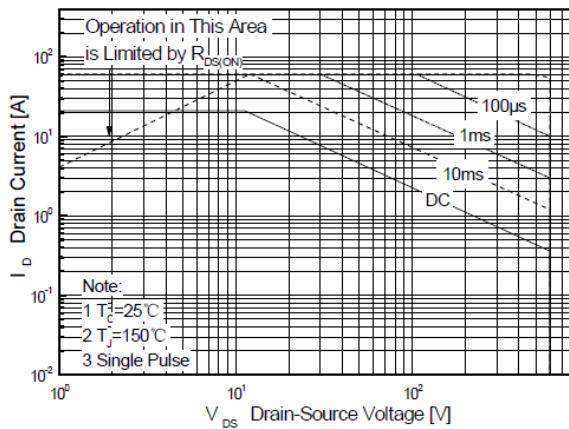


Figure 9-2. Maximum Safe Operating Area

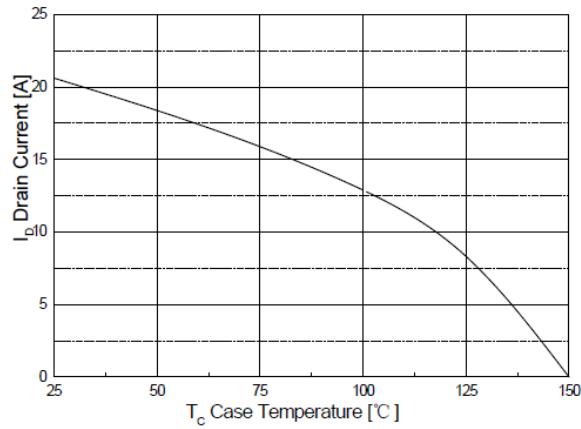


Figure 10. Maximum Drain Current
vs Case Temperature

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Typical Characteristics



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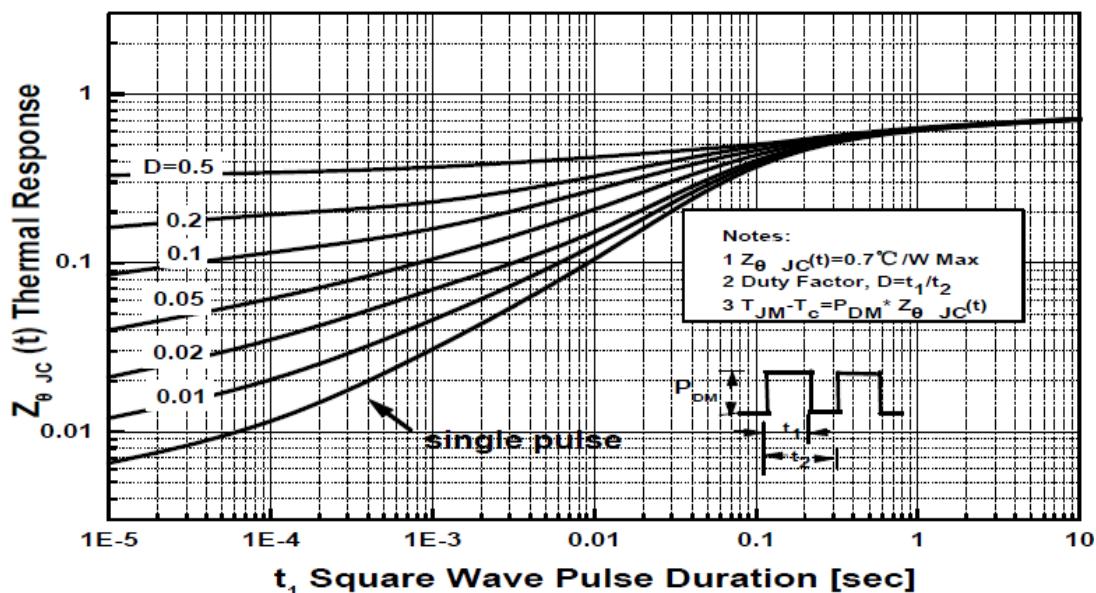


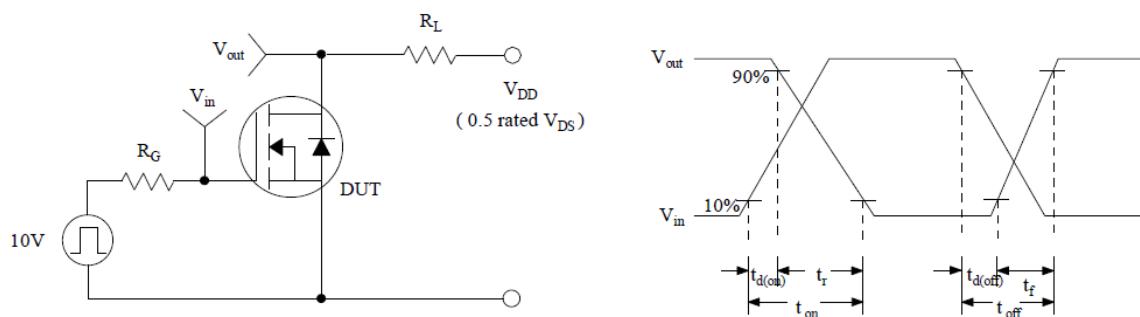
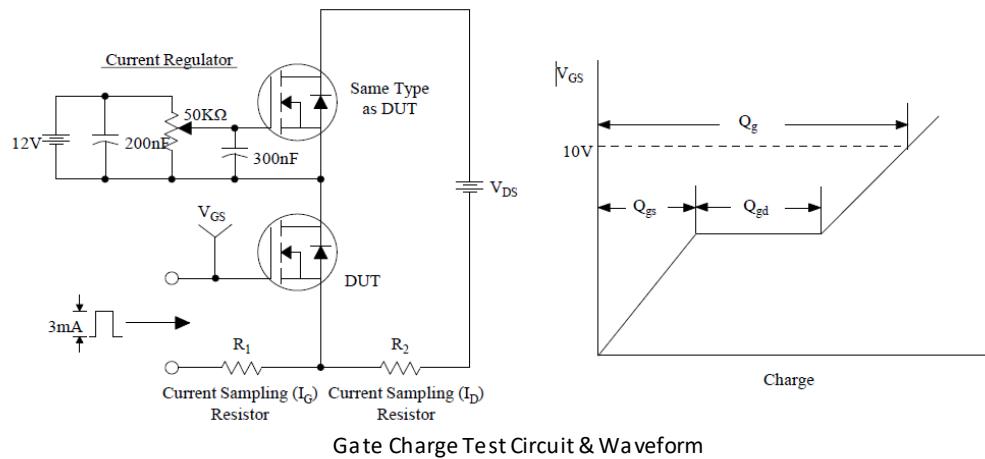
Figure 11-2. Transient Thermal Response Curve for JFAM20N50C

Test Circuit & Waveform

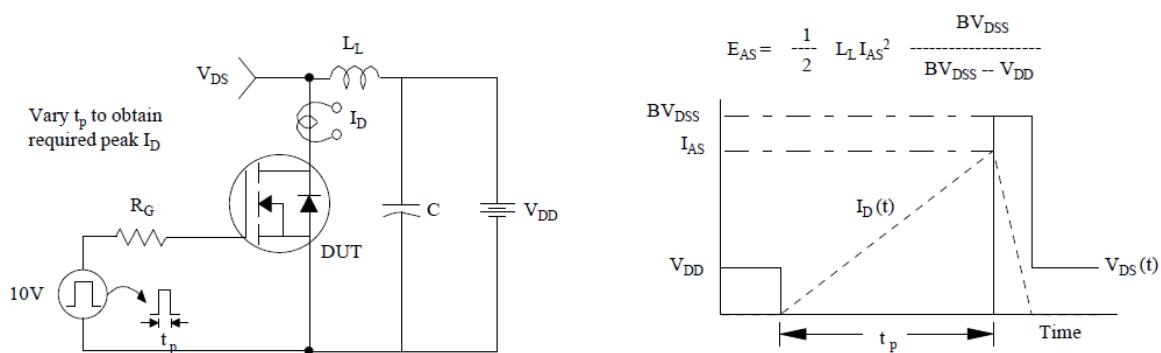


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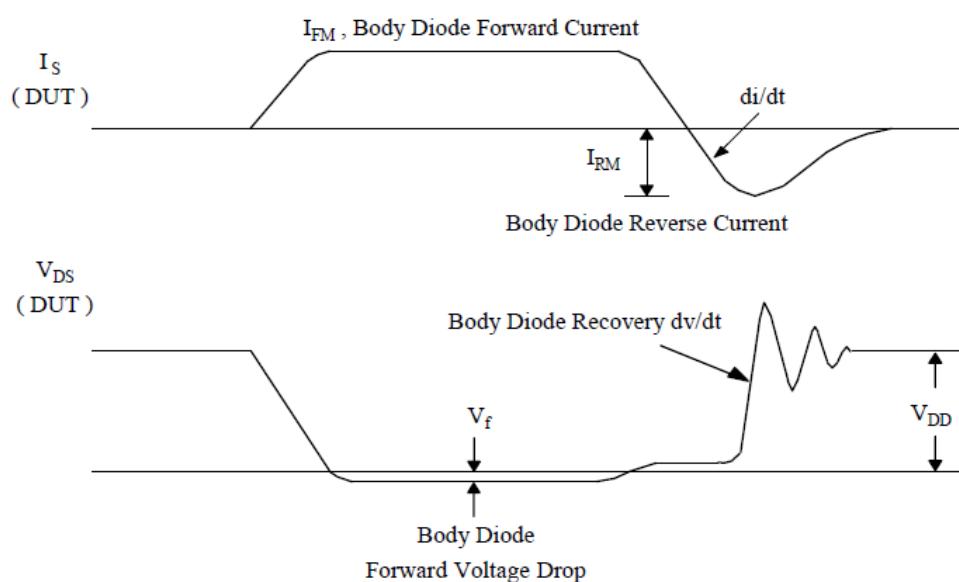
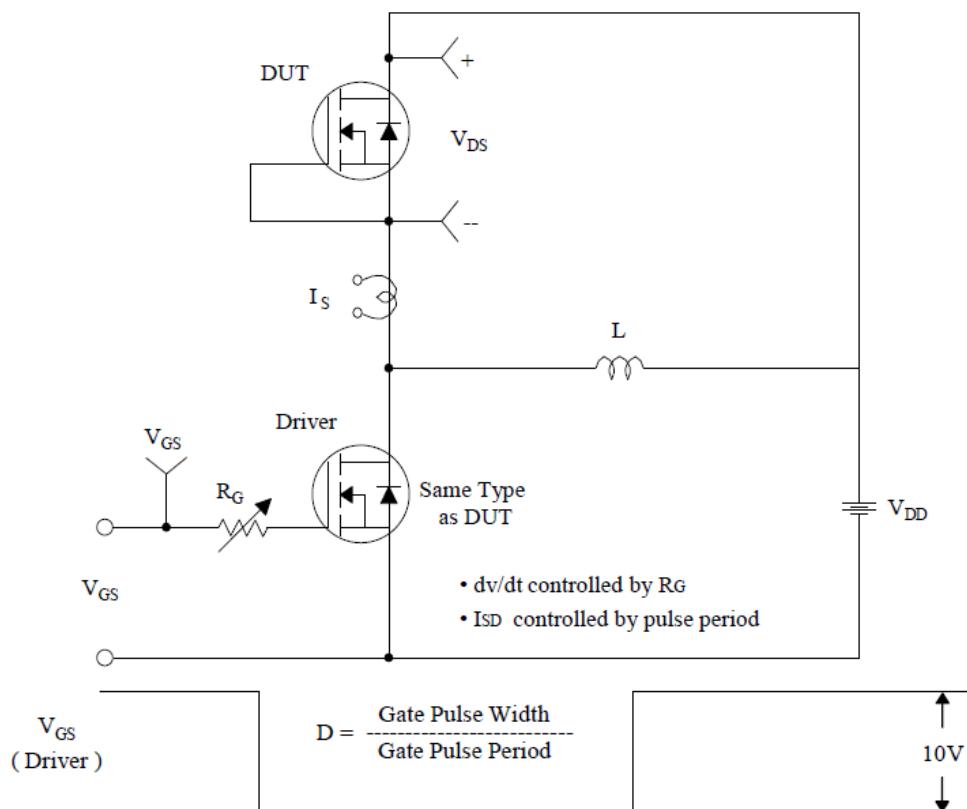


Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

Test Circuit & Waveform

Peak Diode Recovery dv/dt Test Circuit & Waveforms